REMARKS

This is in response to the Office Action mailed on August 27, 2004. Claim 63 is amended to correct a typographical error that resulted in omitting the term "diode" when referring to the n/i/p diode. No claims are added or canceled herein. Thus, claims 1-100 remain pending. Of these pending claims, claims 80-100 stand withdrawn from further consideration.

Supplemental Information Disclosure Statement

Applicant submits a Supplemental Information Disclosure Statement along with a 1449 form herewith, and respectfully requests that a copy of this 1449 Form, with the references marked as being considered and initialed by the Examiner, be returned with the next official communication

§103 Rejection of the Claims

Claims 1-5 and 54-71 were rejected under 35 USC § 103(a) as being unpatentable over Han (U.S. 6,611,452) in view of Babcock et al. (U.S. 6,660,616). Applicant respectfully traverses for at least the following reasons.

In the interest of furthering prosecution of these claims to finality, Applicant responds to the rejection as it is currently understood. However, should the Examiner choose to maintain the rejection, Applicant respectfully requests clarification of the rejection, by clearly stating the reasons for the rejection, and providing such information or references as may be useful in aiding Applicant to judge the propriety of continuing in the prosecution of these claims. (*See* 37 CFR §1.104(a)(2)). Specifically, should the rejection be maintained, Applicant respectfully requests the Examiner to: (1) cite specific portions of the references against every element of the rejected claims, and (2) cite a specific portion of at least one of the references to support a motivation to combine the references.

The rejection stated: *"Han fails to disclose the required intrinsic region requirement."* The rejection further stated: *"It would have been obvious to one of having* (sic) *ordinary skill in the art at the time the invention was made to include the required intrinsic region configuration in Han as taught by Babcock et al. in order to have a memory cell with higher performance."* (emphasis added).

Applicant respectfully submits that the rejection fails to provide a proper motivation to combine the references. The TCCT based memory cell of Han appears to be based on the cell disclosed by Nemati et al. (col. 1 lines 13-32), which includes a P+/N/P/N+ thyristor structure (Fig. 2). The rejection does not identify where the intrinsic region of Babcock et al. would be included in this thyristor structure, and does not support the assertion that the intrinsic region would provide the memory cell with higher performance with a citation to the references. Applicant is unable to find a fair suggestion in Han to use a diode with an intrinsic region between a cathode and an anode. Furthermore, Babcock et al. relates to a transit time device (Title, Abstract), and identifies advantages in the field of high frequency applications (Col. 1, lines 18-21 and 36-42). Applicant is unable to find a fair suggestion Babcock et al. to use the transit time device with a memory cell. Applicant performed an electronic search of an electronic copy of Babcock et al., and did not find the term "memory".

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. (MPEP §2143). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not in Applicant's disclosure (MPEP §2143, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Applicant respectfully submits that the rejection fails to point out an explicit motivation in the references to combine in the references. Furthermore, Applicant respectfully submits that the rejection fails to provide the evidence necessary to support an implicit motivation to combine the references. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." (MPEP §2143.01, citing *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Lee,* 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) (discussing the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992)).

With respect to independent claim 1, Applicant is unable to find, among other things in the Han and Babcock et al. references, a motivation to combine the references, and a memory cell comprising an access transistor as recited in the claim, and a diode exhibiting Negative Differential Resistance (NDR) behavior connected between the floating node and a diode reference potential line, where the diode includes an anode, a cathode and an intrinsic region between the anode and the cathode, and where the intrinsic region of the diode assists with stabilizing the memory state of the memory cell, as recited in the claim. Claims 2-5 depend on independent claim 1, and are believed to be in condition for allowance at least for the reasons provided with respect to independent claim 1.

With respect to independent claim 54, Applicant is unable to find, among other things in the Han and Babcock et al. references, a motivation to combine the references, and a memory cell comprising and access transistor as recited in the claim, and a Negative Differential Resistance (NDR) p/i/n diode connected between a diode reference potential line and the second diffusion region of the access transistor, where the p/i/n diode includes a p-type anode, an n-type cathode, and an intrinsic region positioned between the anode and the cathode, as recited in the claim. Claims 55-62 depend on independent claim 54, and are believed to be in condition for allowance at least for the reasons provided with respect to independent claim 54.

With respect to independent claim 63, Applicant is unable to find, among other things in the Han and Babcock et al. references, a motivation to combine the references, and a memory cell comprising an access transistor as recited in the claim, and a Negative Differential Resistance (NDR) n/i/p diode connected between a diode reference potential line and the second diffusion region, where the n/i/p diode includes an n-type anode, a p-type cathode, and an intrinsic region positioned between the anode and the cathode, as recited in the claim. Claims 64-71 depend on independent claim 63, and are believed to be in condition for allowance at least for the reasons provided with respect to independent claim 63.

Thus, Applicant respectfully requests withdrawal of the rejections, and reconsideration and allowance of the claims.

Reservation of Rights

Applicant maintains its right to swear behind any references relied upon for a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the documents are prior art.

Allowable Subject Matter

Claims 6-53 and 72-79 were allowed.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6960 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 11-29-04

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29 day of November, 2004.

KACIA LEE
Name

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Signature